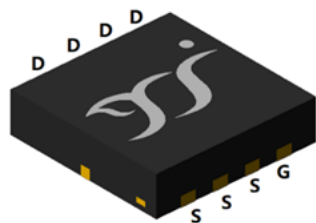
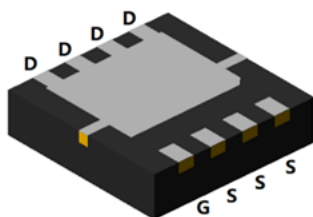




N-Channel Enhancement Mode Field Effect Transistor

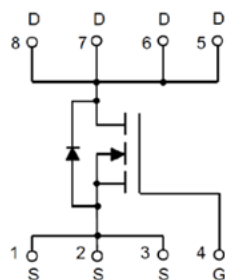


Top View



Bottom View

DFN3333-8L



Product Summary

- V_{DS} 40 V
- I_D 20 A
- $R_{DS(ON)}$ (at $V_{GS}=10V$) <14.0 mohm
- $R_{DS(ON)}$ (at $V_{GS}=4.5V$) <18.5 mohm
- 100% EAS Tested
- 100% ∇V_{DS} Tested
- ESD Level (HBM) Class 1B

General Description

- Trench Power LV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- High current load applications
- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	40	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_C=25^\circ\text{C}$	I_D	20	A
	$T_C=100^\circ\text{C}$		14	
Pulsed Drain Current ^A		I_{DM}	90	A
Single Pulse Avalanche Energy ^B		E_{AS}	70	mJ
Total Power Dissipation	$T_C=25^\circ\text{C}$	P_D	21	W
	$T_A=25^\circ\text{C}$		2.34	
Thermal Resistance Junction-to-Case		$R_{\theta JC}$	5.9	$^\circ\text{C/W}$
		$R_{\theta JA}$	53.4	
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ\text{C}$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJQ20N04A	F1	Q20N04	5000	10000	100000	13" reel



YJQ20N04A

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	40			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =40V, V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1.0	1.5	2.5	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D =20A		11	14	mΩ
		V _{GS} = 4.5V, I _D =10A		14.3	18.5	
Diode Forward Voltage	V _{SD}	I _S =10A, V _{GS} =0V		0.7	1.2	V
Maximum Body-Diode Continuous Current	I _S				20	A
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =20V, V _{GS} =0V, f=1MHZ		917		pF
Output Capacitance	C _{oss}			128		
Reverse Transfer Capacitance	C _{rss}			108		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =20V, I _D =20A		23.6		nC
Gate-Source Charge	Q _{gs}			4.4		
Gate-Drain Charge	Q _{gd}			6.3		
Reverse Recovery Charge	Q _{rr}	I _F =20A, di/dt=100A/us		0.4		
Reverse Recovery Time	t _{rr}			7		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =20V, I _D =2A, R _{GEN} =3Ω		10		ns
Turn-on Rise Time	t _r			56		
Turn-off Delay Time	t _{D(off)}			27		
Turn-off fall Time	t _f			72		

A. Pulse Test: Pulse Width≤300us, Duty cycle ≤2%.

B. R_{θJA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{θJC} is guaranteed by design, while R_{θJA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



■ Typical Performance Characteristics

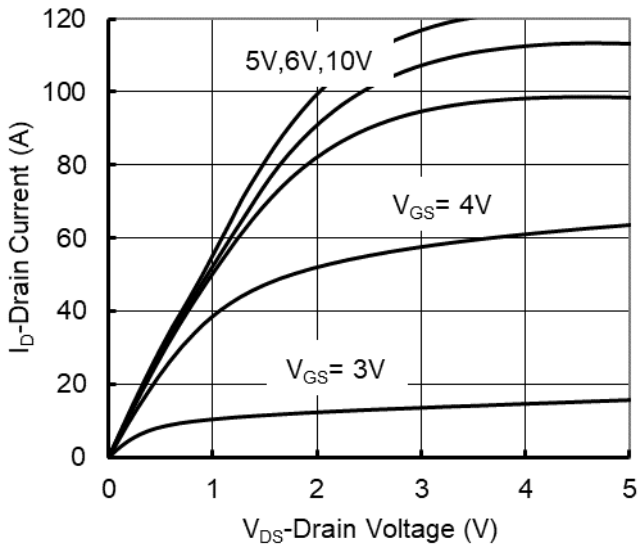


Figure 1. Output Characteristics

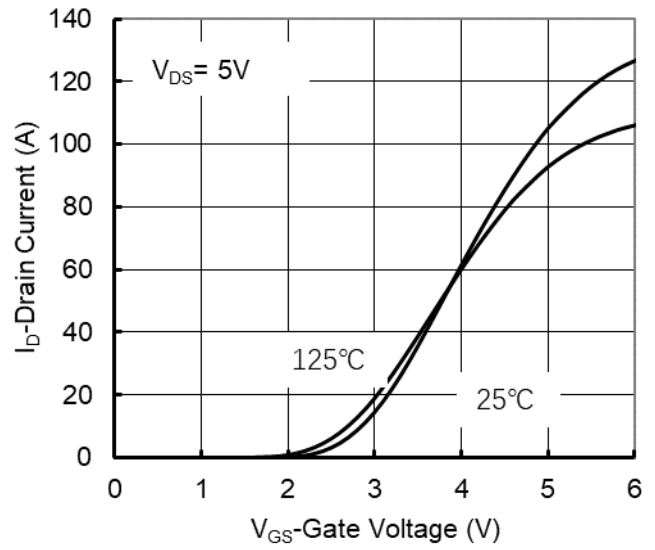


Figure 2. Transfer Characteristics

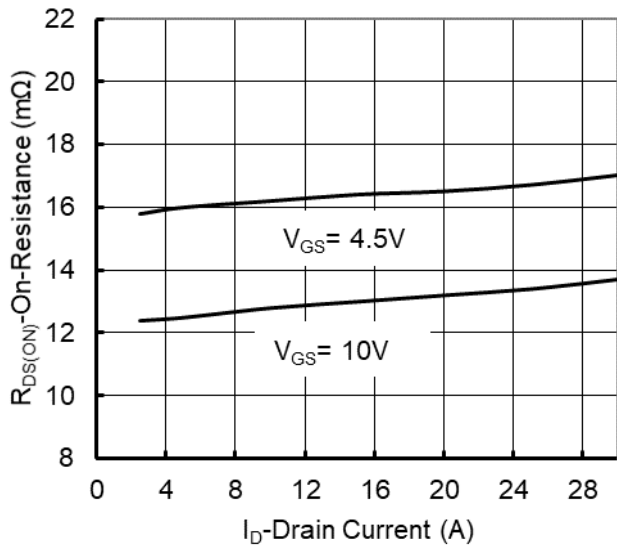


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

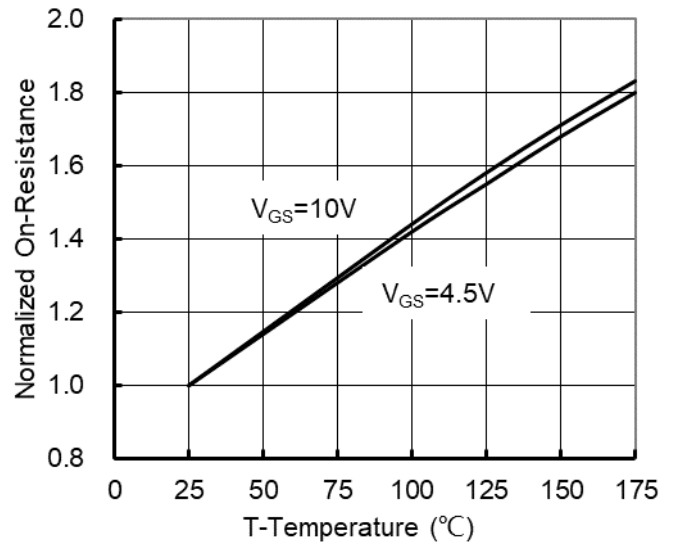


Figure 4. On-Resistance vs. Junction Temperature

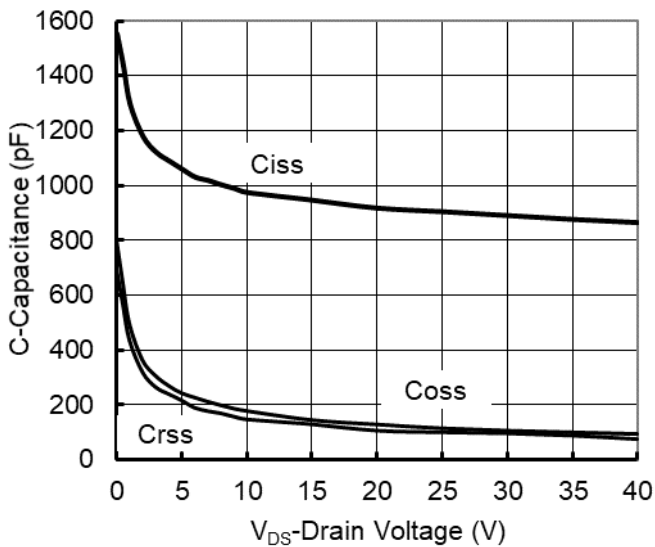


Figure 5. Capacitance Characteristics

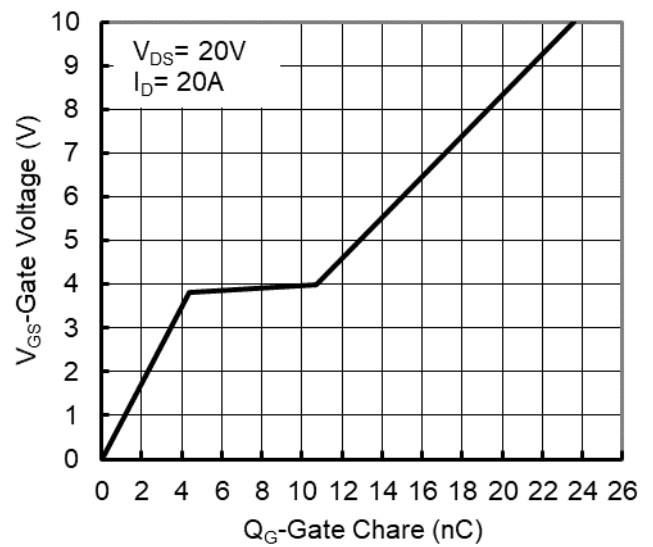


Figure 6. Gate Charge

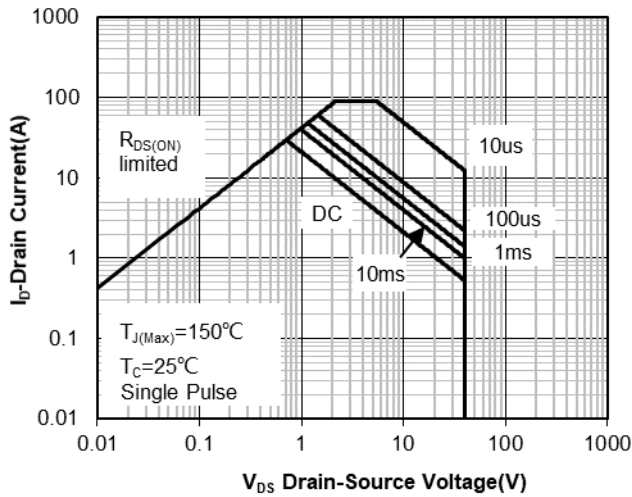


Figure 7. Safe Operation Area

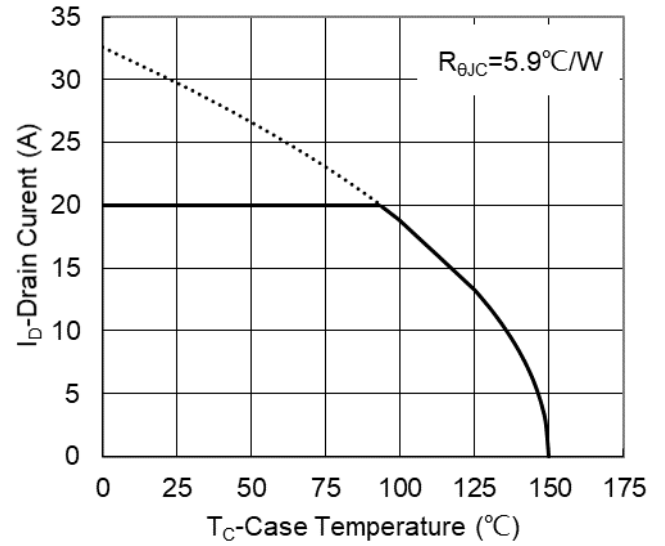


Figure 8. Maximum Continuous Drain Current vs Case Temperature

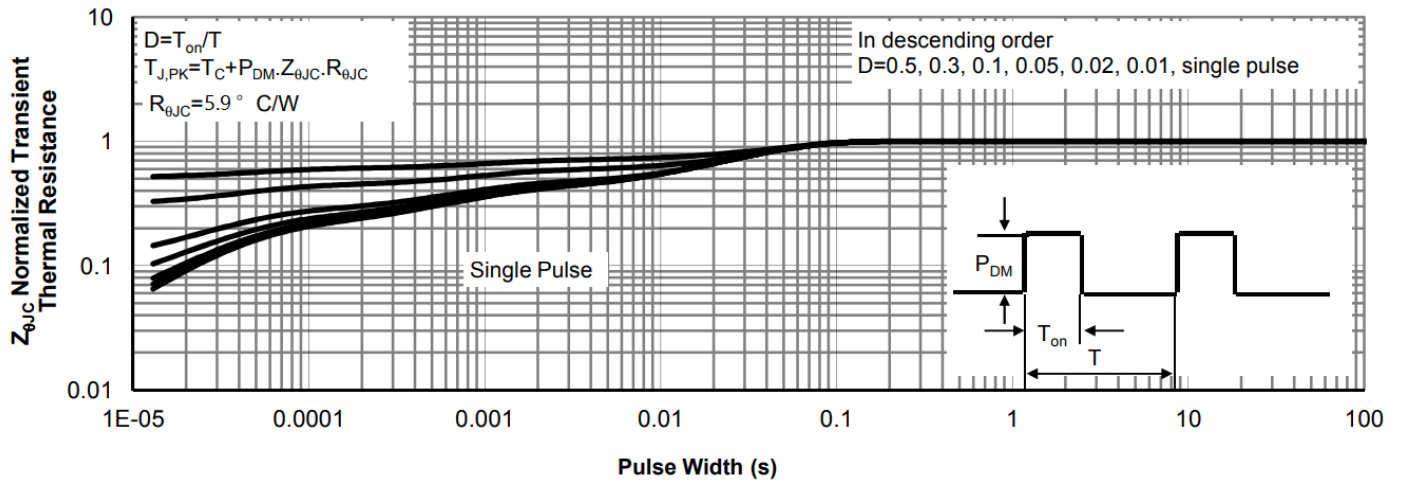
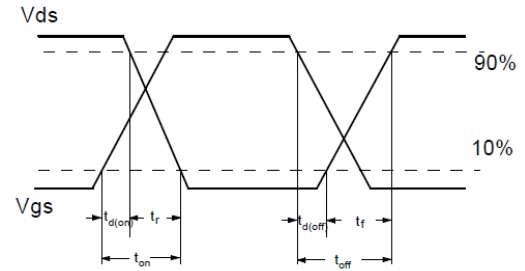
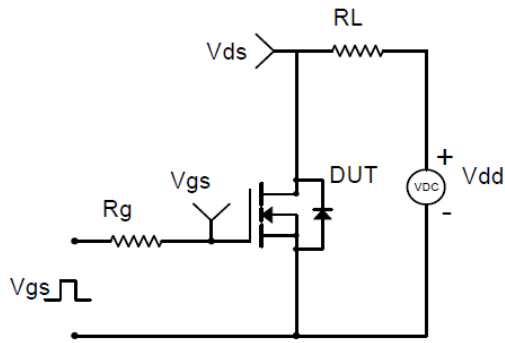
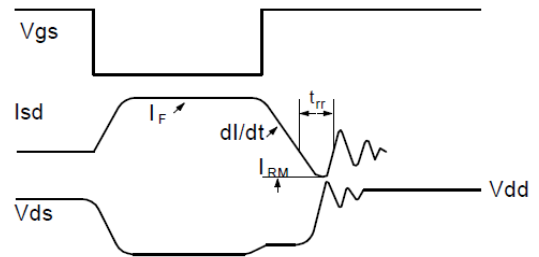
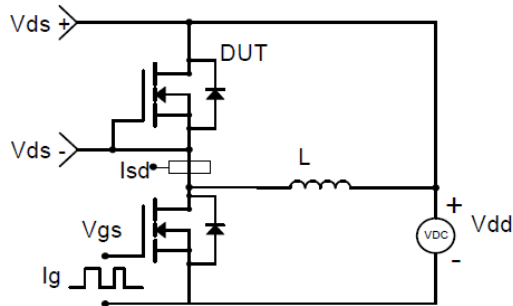


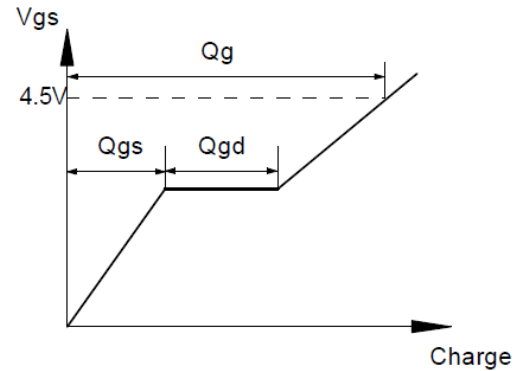
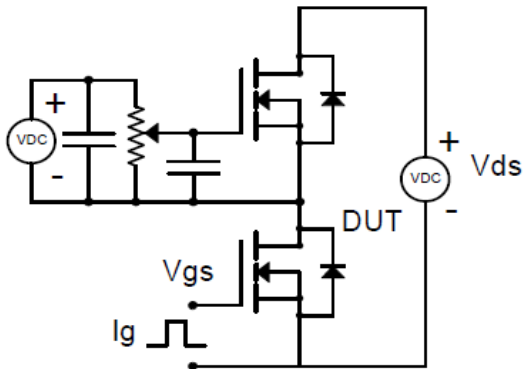
Figure 9. Normalized Maximum Transient Thermal Impedance



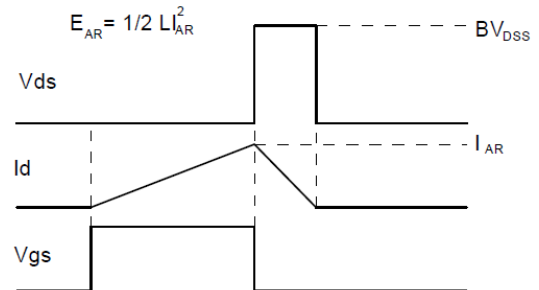
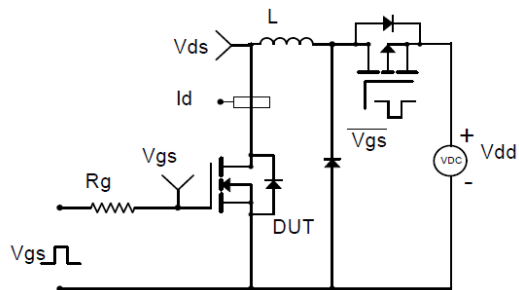
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Gate Charge Test Circuit & Waveform



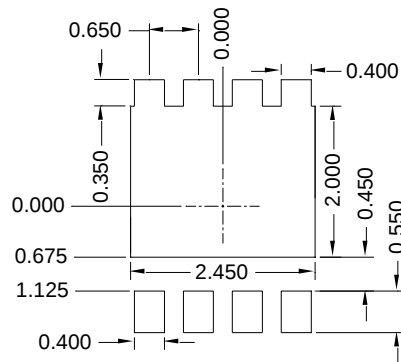
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Technical drawing of a rectangular plate. The drawing shows two views: a front view (left) and a side view (right). The front view is a rectangle with dimensions D (width) and E (height). The side view shows the plate's profile with dimensions $D1$ (width of the top flange), $L2$ (total height), $L3$ (height of the top flange), $L4$ (height of the bottom flange), $E1$ (height of the main body), 1×4 (height of the bottom flange), e (width of the bottom flange), and $bx8$ (width of the bottom flange).

Bottom View
背面视图

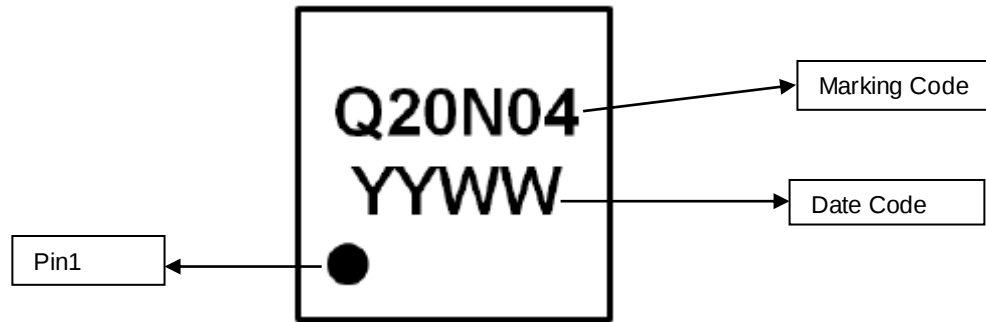
Side View
侧面视图



Suggested Solder Pad Layout
Top View

1. Controlling dimension: in millimeters.
2. General tolerance: $\pm 0.10\text{mm}$.
3. The pad layout is for reference purposes only.

■ Marking Information



Note:

1. All marking is at middle of the product body
2. All marking is in laser printing
3. Q20N04 is marking code, YYWW is date code, "YY" is year, "WW" is week
4. Body color: Black



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