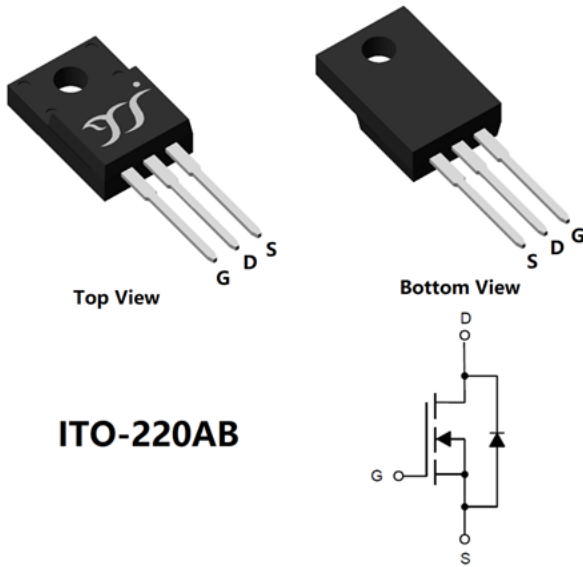


N-Channel Enhancement Mode Field Effect Transistor



Product Summary

• V_{DS}	100V
• I_D	95A
• $R_{DS(ON)}$ (at $V_{GS}=10V$)	$<3.3m\Omega$
• 100% EAS Tested	
• 100% ∇V_{DS} Tested	

General Description

- Split Gate Trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Load switch
- Battery management
- Solar

Limiting Values

Parameter	Conditions		Symbol	Min	Max	Unit
Drain-source Voltage			V _{DS}	-	100	V
Gate-source Voltage			V _{GS}	-20	20	
Continuous Drain Current (Note 1,2)	Steady-State	T _A =25°C,V _{GS} =10V	I _D	-	17	A
		T _A =100°C,V _{GS} =10V		-	12	
Continuous Drain Current (Note 1,3)	Steady-State	T _C =25°C,V _{GS} =10V,Chip limitation		-	95	
		T _C =100°C,V _{GS} =10V		-	67	
Pulsed Drain Current	T _C =25°C,t _p ≤10μs		I _{DM}	-	380	
Maximum Body-Diode Continuous Current	T _C =25°C		I _S		63	
Avalanche Energy (non-repetitive)	T _J =25°C,V _G =10V,R _G =25Ω,L=0.5mH,I _{AS} =50A		EAS	-	625	mJ
Total Power Dissipation (Note 1,2)	Steady-State	T _A =25°C	P _D	-	2	W
		T _A =100°C		-	1	
Total Power Dissipation (Note 1,3)	Steady-State	T _C =25°C		-	62.5	
		T _C =100°C		-	31.2	
Junction and Storage Temperature Range			T _J , T _{STG}	-55	175	°C

Thermal Resistance

Parameter		Symbol	Typ	Max	Units
Thermal Resistance Junction-to-Ambient (Note 2)	Steady-State	$R_{\theta JA}$	-	75	$^{\circ}C/W$
Thermal Resistance Junction-to-Case	Steady-State	$R_{\theta JC}$	-	2.4	

Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJF3D3G10H	B1	YJF3D3G10H	50	/	5000	Tube



YJF3D3G10H

■ Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA, T _j =25℃	100	-	-	V
		V _{GS} =0V, I _D =1mA, T _j =25℃	100	-	-	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =100V, V _{GS} =0V, T _j =25℃	-	-	1	μA
		V _{DS} =100V, V _{GS} =0V, T _j =125℃	-	-	100	
Gate-Source Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V, T _j =25℃	-	-	±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA, T _j =25℃	2.1	2.9	3.7	V
Static Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =10V, I _D =50A, T _j =25℃	-	2.5	3.3	mΩ
Diode Forward Voltage	V _{SD}	I _S =50A, V _{GS} =0V, T _j =25℃	-	0.86	1.2	V
Gate Resistance	R _G	f=1MHz, T _j =25℃	-	2.3	-	Ω
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =50V, V _{GS} =0V, f=0.5MHz, T _j =25℃	-	7076	-	pF
Output Capacitance	C _{oss}		-	2348	-	
Reverse Transfer Capacitance	C _{rss}		-	42	-	
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =50V, I _D =50A, T _j =25℃	-	94	-	nC
Gate-Source Charge	Q _{gs}		-	30.5	-	
Gate-Drain Charge	Q _{gd}		-	15	-	
Reverse Recovery Charge	Q _{rr}	I _F =50A, di/dt=100A/μs, V _{GS} =0V, V _R =50V, T _j =25℃	-	50	-	nC
Reverse Recovery Time	t _{rr}		-	48	-	ns
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DS} =50V, I _D =50A, R _L =1Ω, R _{GEN} =3Ω, T _j =25℃	-	29	-	ns
Turn-on Rise Time	t _r		-	54	-	
Turn-off Delay Time	t _{D(off)}		-	67	-	
Turn-off Fall Time	t _f		-	42	-	

- Note:
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
 2. The value of $R_{\theta JA}$ is measured in the still air environment with $T_A=25^\circ C$. The maximum allowed junction temperature of $175^\circ C$.
 3. Thermal resistance from junction to soldering point (on the exposed drain pad).



■ Typical Electrical and Thermal Characteristics Diagrams

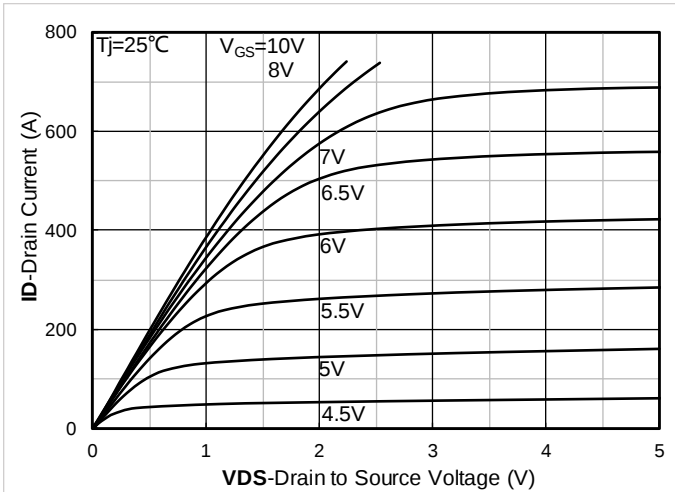


Figure 1. Output Characteristics; typical values

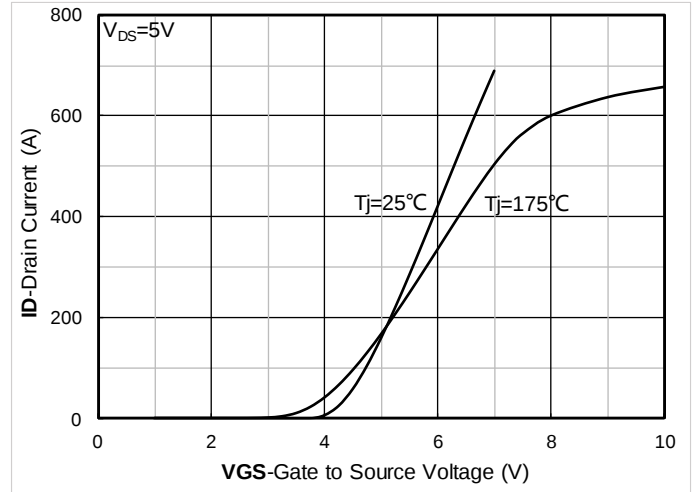


Figure 2. Transfer Characteristics; typical values

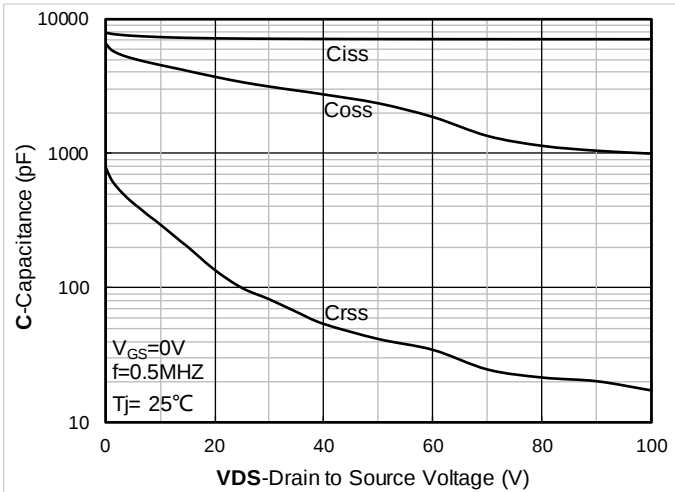


Figure 3. Capacitance Characteristics; typical values

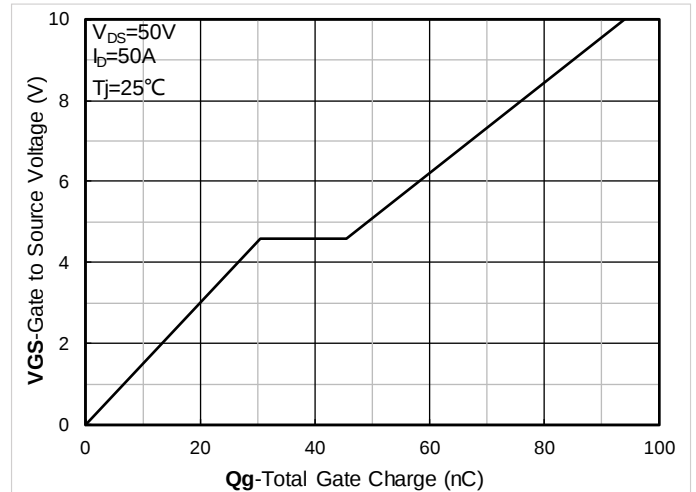


Figure 4. Gate Charge; typical values

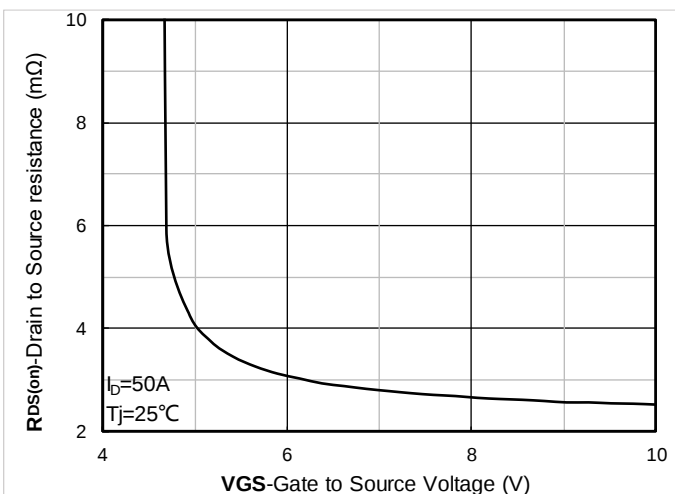


Figure 5. On-Resistance vs. Gate to Source Voltage; typical values

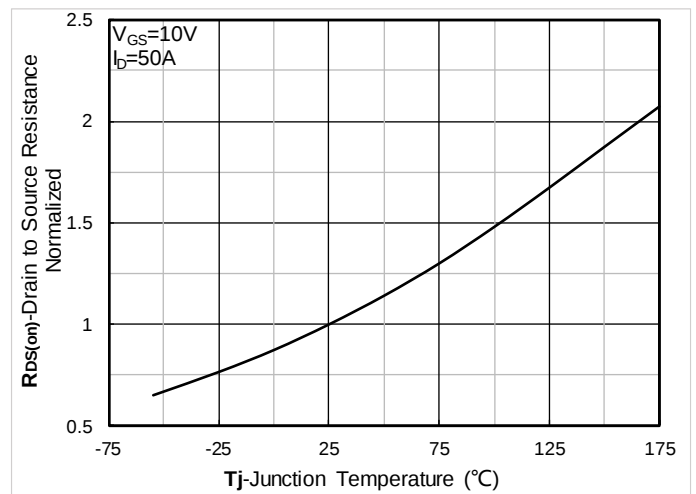


Figure 6. Normalized On-Resistance

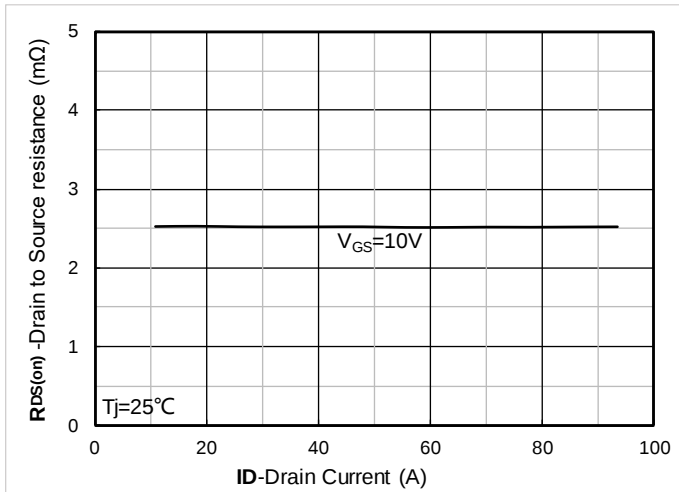


Figure 7. $R_{DS(on)}$ vs. Drain Current; typical values

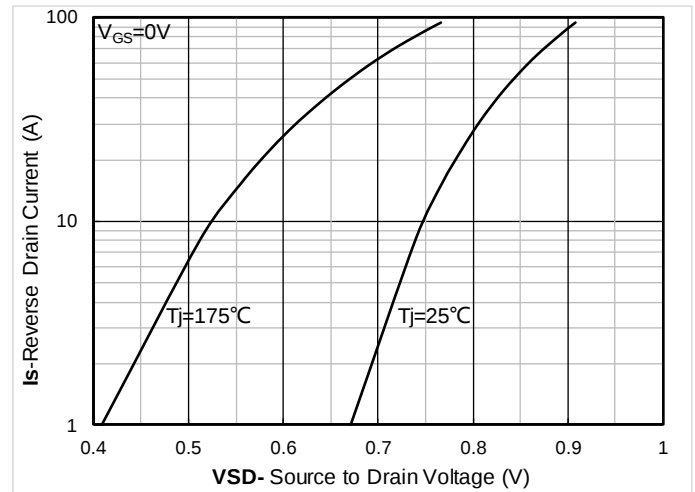


Figure 8. Forward characteristics of reverse diode; typical values

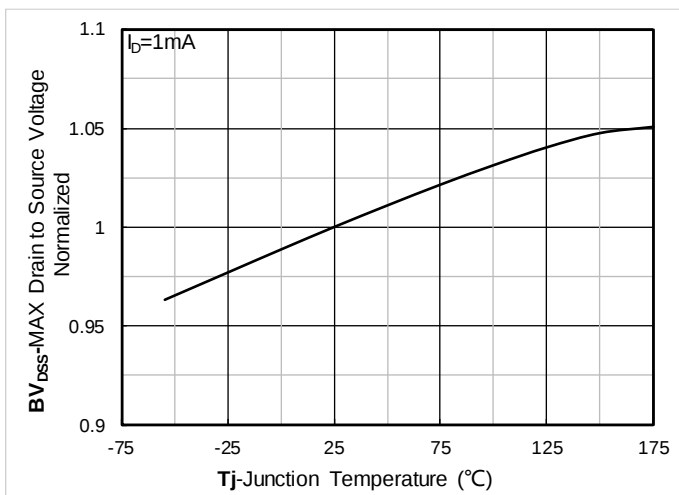


Figure 9. Normalized breakdown voltage

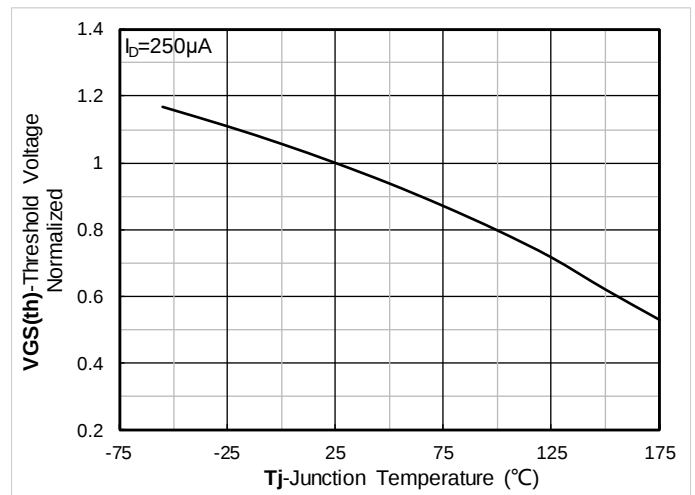


Figure 10. Normalized Threshold voltage

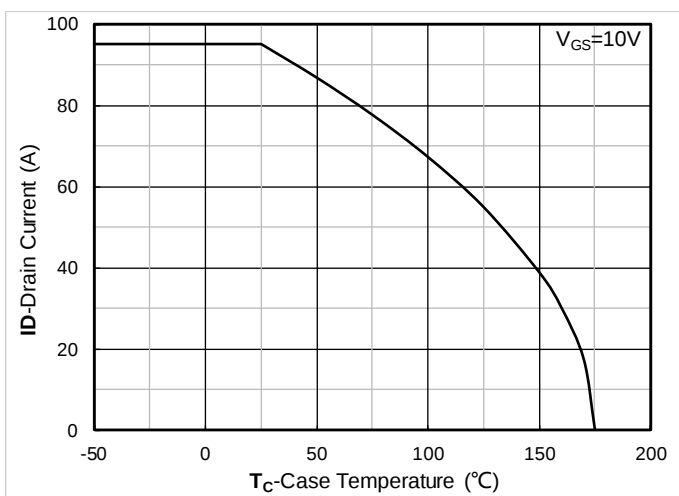


Figure 11. Current dissipation

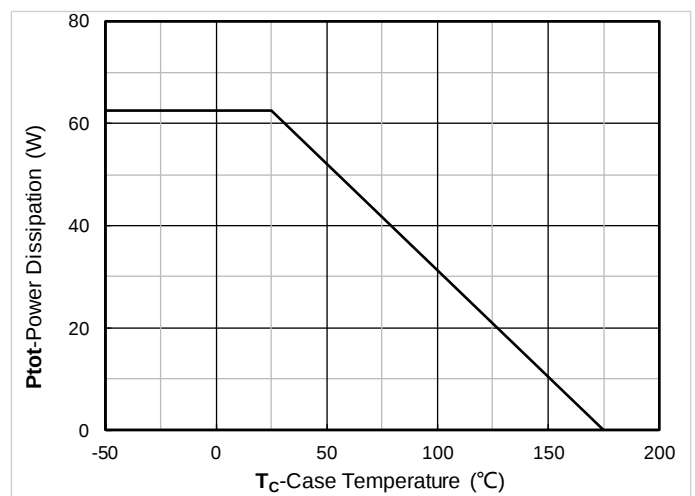


Figure 12. Power dissipation

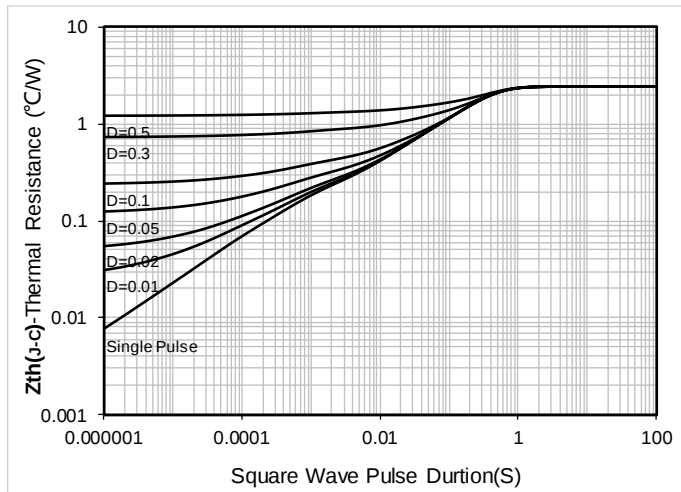


Figure 13. Maximum Transient Thermal Impedance

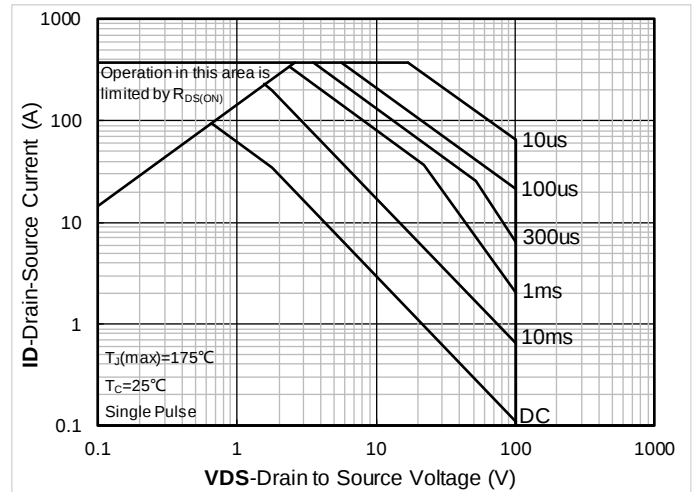


Figure 14. Safe Operation Area

■ Test Circuits & Waveforms

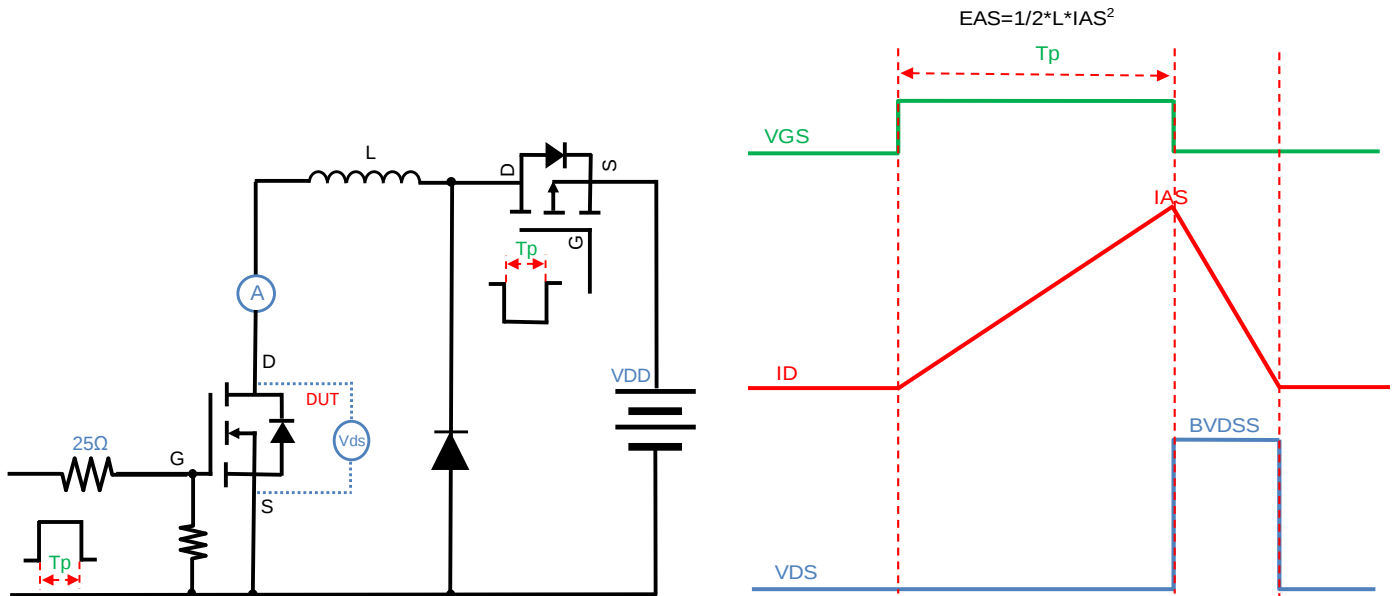


Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

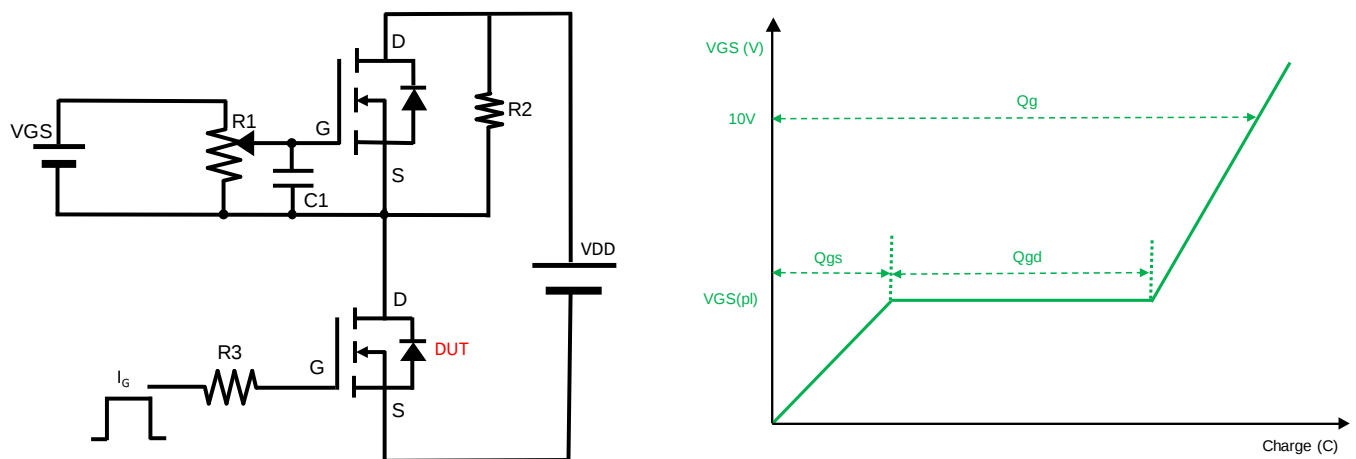


Figure B. Gate Charge Test Circuit & Waveform

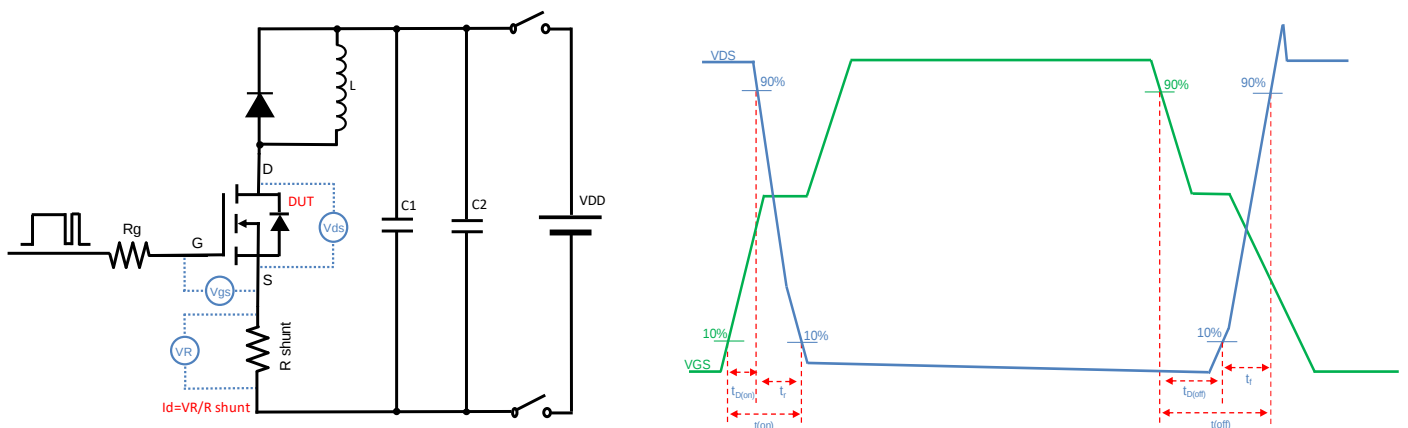


Figure C. Resistive Switching Test Circuit & Waveform

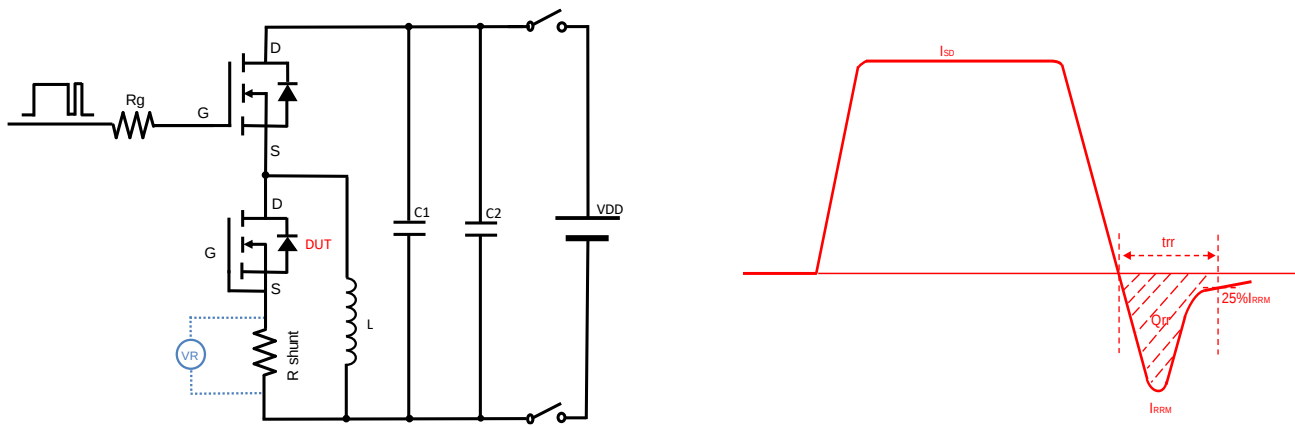
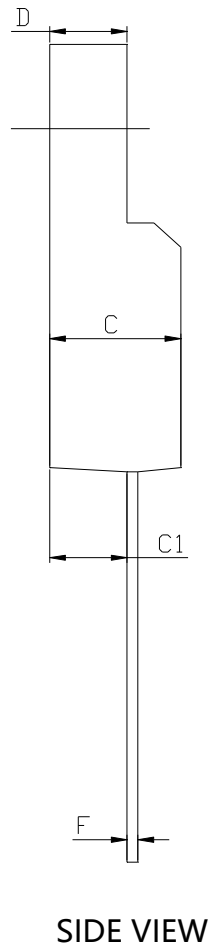
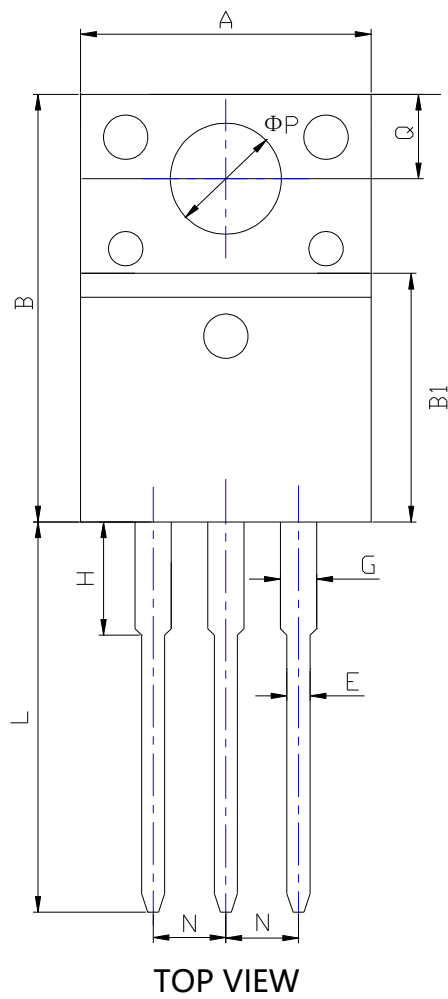


Figure D. Diode Recovery Test Circuit & Waveform



YJF3D3G10H

■ ITO-220AB-C Package Information



SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.382	0.406	9.700	10.300
B	0.610	0.634	15.500	16.100
B1	0.354	0.370	8.990	9.390
C	0.177	0.193	4.500	4.900
C1	0.102	0.116	2.600	2.950
D	0.092	0.108	2.340	2.740
E	0.028	0.035	0.700	0.900
F	0.016	0.024	0.400	0.600
G	0.044	0.056	1.120	1.420
H	0.106	0.126	2.700	3.200
L	0.496	0.535	12.600	13.600
N	0.092	0.108	2.340	2.740
Q	0.124	0.140	3.150	3.550
ΦP	0.118	0.130	3.000	3.300

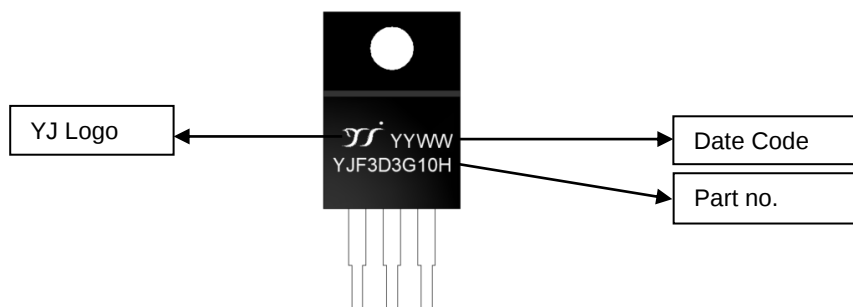
NOTE:

- 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
- 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.



YJF3D3G10H

■ Marking Information



Note:

1. All marking is at middle of the product body
2. All marking is in laser printing
3. YJF3D3G10H is part no., YYWW is date code, "YY" is year, "WW" is week
4. Body color: Black



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