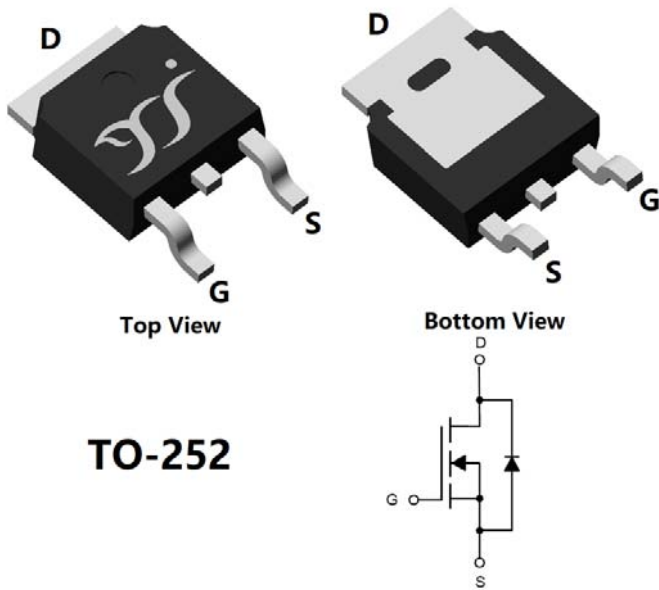


N-Channel Enhancement Mode Field Effect Transistor



TO-252

Product Summary

• V_{DS}	60 V
• I_D	50 A
• $R_{DS(ON)}$ (at $V_{GS}=10V$)	< 15 mohm
• $R_{DS(ON)}$ (at $V_{GS}=4.5V$)	< 17 mohm
• 100% EAS Tested	
• 100% ∇V_{DS} Tested	
• ESD Level(HBM)	Class 1C

General Description

- Trench Power MV MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- DC-DC Converters
- Power management functions
- Motor Drive applications

■ Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source Voltage		V_{DS}	60	V
Gate-source Voltage		V_{GS}	± 20	V
Drain Current	$T_C=25^\circ\text{C}$	I_D	50	A
	$T_C=100^\circ\text{C}$		42	
Pulsed Drain Current ^A		I_{DM}	200	A
Total Power Dissipation @ $T_C=25^\circ\text{C}$ ^B		P_D	54	W
Total Power Dissipation @ $T_C=100^\circ\text{C}$ ^B		P_D	21.6	W
Total Power Dissipation @ $T_A=25^\circ\text{C}$ ^C		P_D	6.2	W
Single Pulse Avalanche Energy ^D		E_{AS}	49	mJ
Thermal Resistance Junction-to-Case		$R_{\theta JC}$	2.3	$^\circ\text{C}/\text{W}$
Thermal Resistance Junction-to-Ambient		$R_{\theta JA}$	20	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range		T_J, T_{STG}	-55~+150	$^\circ\text{C}$

■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	Marking	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
YJD50N06A	F1/F2	YJD50N06A	2500	/	25000	13" reel



YJD50N06A

■ Electrical Characteristics (T_J=25℃ unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} = 0V, I _D =250μA	60			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =60V,V _{GS} =0V			1	μA
Gate-Body Leakage Current	I _{GSS}	V _{GS} = ±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250μA	1.0	1.5	2.5	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D =15A		11	15	mΩ
		V _{GS} = 4.5V, I _D =10A		13.5	17	
Diode Forward Voltage	V _{SD}	I _S =15A,V _{GS} =0V		0.80	1.2	V
Maximum Body-Diode Continuous Current	I _S				50	A
Gate resistance	R _g	f=1 MHz		2.1		Ω
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =30V,V _{GS} =0V,f=1MHZ		2585		pF
Output Capacitance	C _{oss}			150		
Reverse Transfer Capacitance	C _{rss}			77.5		
Switching Parameters						
Total Gate Charge	Q _g (10V)	V _{GS} =10V,V _{DS} =30V,I _D =20A		51		nC
Total Gate Charge	Q _g (4.5V)			24		
Gate-Source Charge	Q _{gs}			9.5		
Gate-Drain Charge	Q _{gd}			10		
Reverse Recovery Charge	Q _{rr}	I _F =20A, di/dt=100A/us		17		ns
Reverse Recovery Time	t _{rr}			14		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DD} =30V , I _D =20A R _{GEN} =3Ω		11		
Turn-on Rise Time	t _r			25		
Turn-off Delay Time	t _{D(off)}			89		
Turn-off fall Time	t _f			79		

A. Pulse Test: Pulse Width≤300us, Duty cycle ≤2%.

B. The power dissipation P_D is based on T_{J(MAX)}=150℃, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. The value of R_{θJA} is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25℃.

D. T_J=25℃, V_{DD}=55V, V_G=10V, L=0.5mH.



■ Typical Performance Characteristics

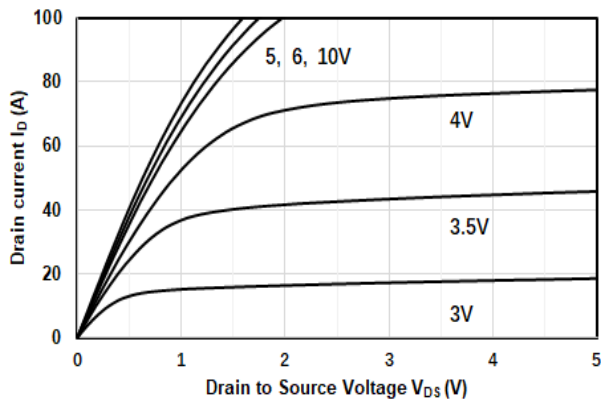


Figure1. Output Characteristics

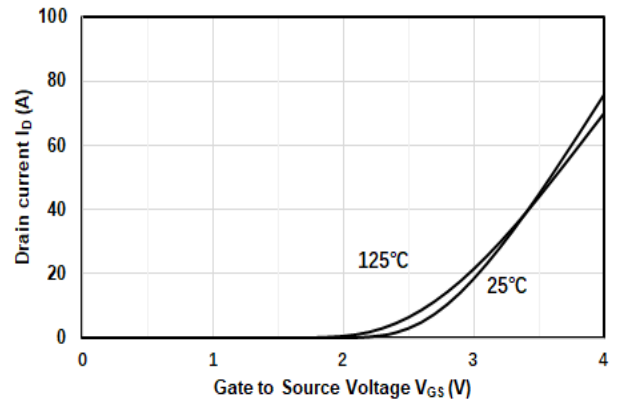


Figure2. Transfer Characteristics

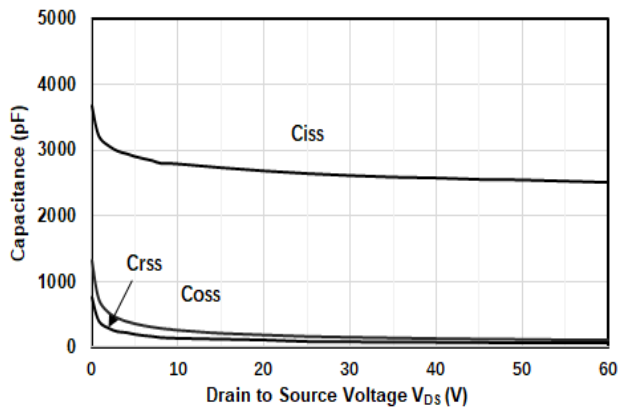


Figure3. Capacitance Characteristics

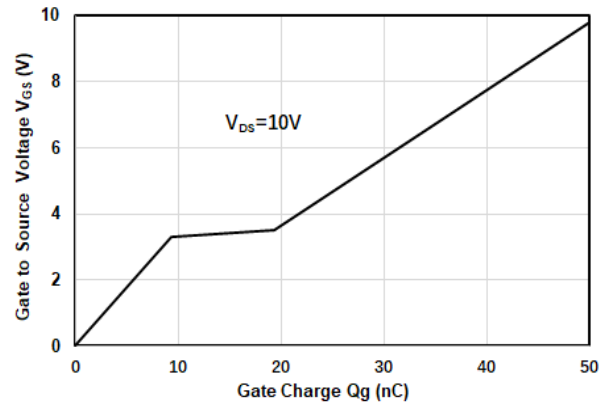


Figure4. Gate Charge

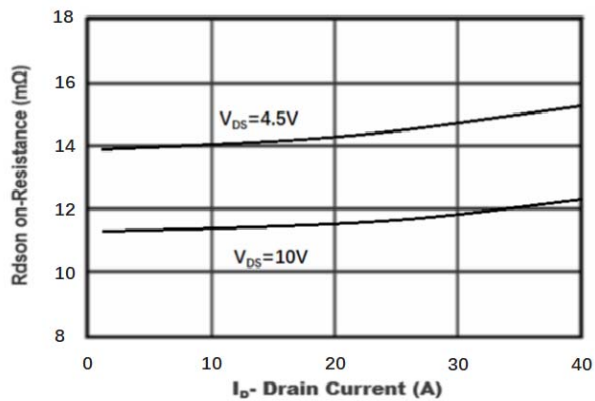


Figure5. Drain-Source on Resistance

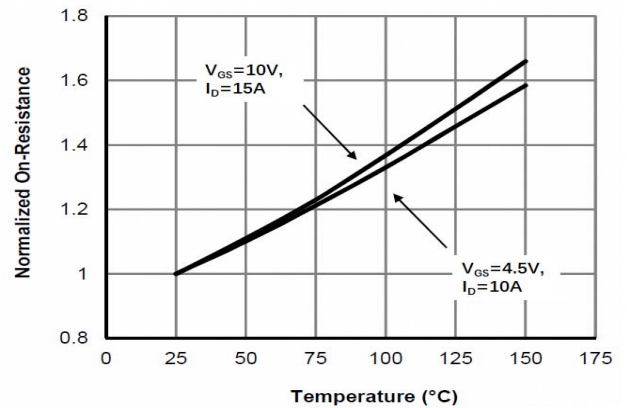


Figure6. Drain-Source on Resistance



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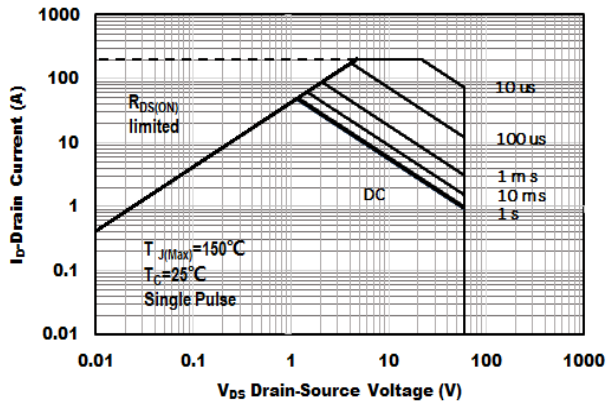


Figure7. Safe Operation Area

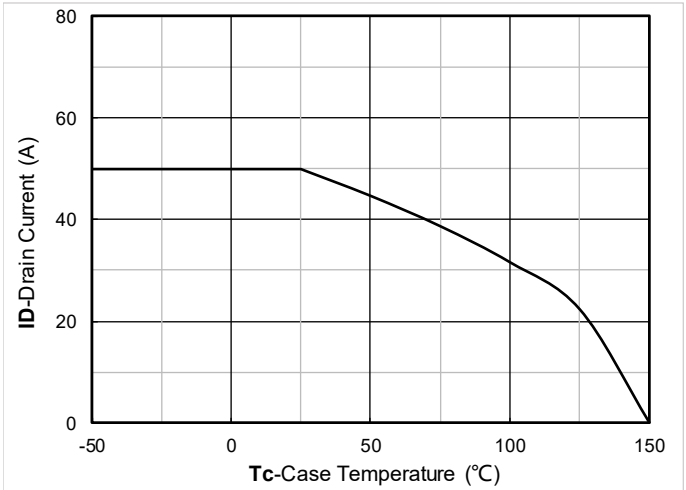


Figure8. Drain current vs. Case Temperature

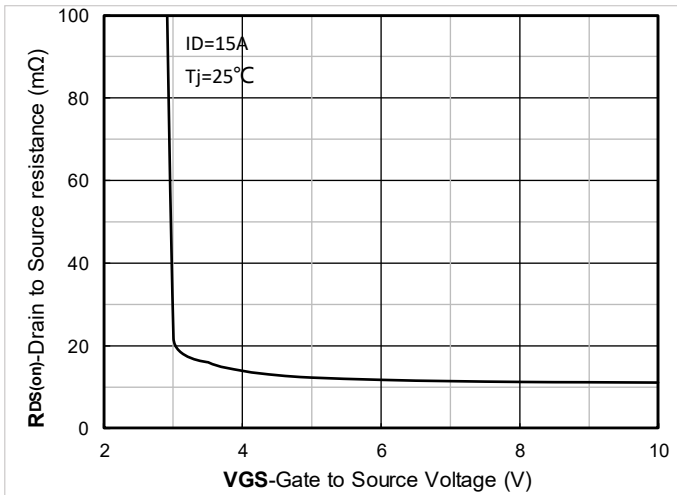


Figure 9. On-Resistance vs Gate to Source Voltage

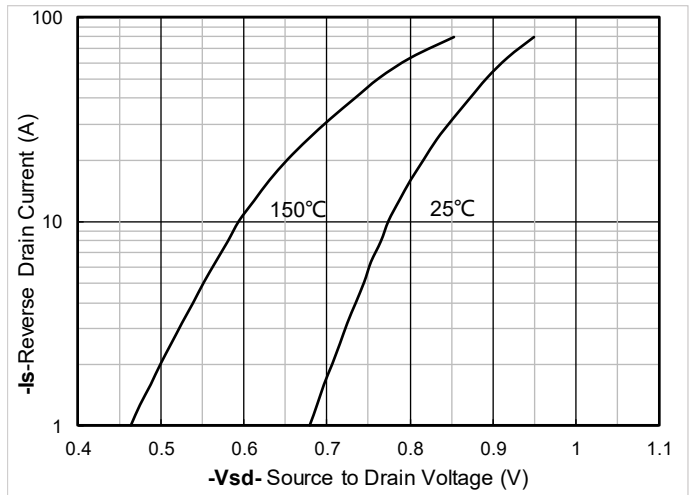


Figure 10. Forward characteristics of reverse diode

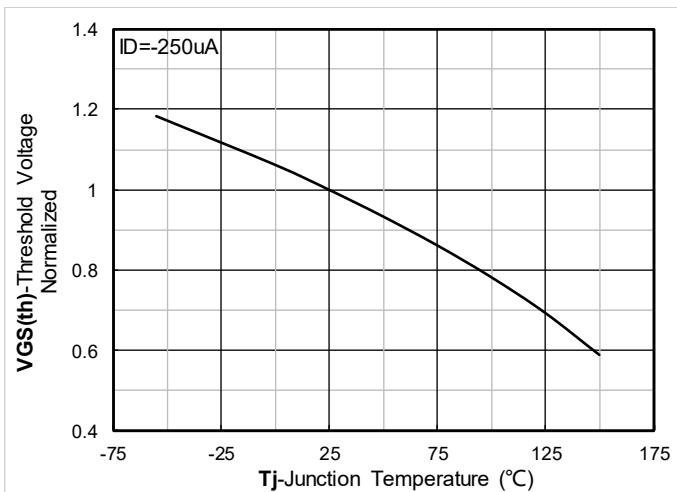


Figure 11. Normalized Threshold voltage

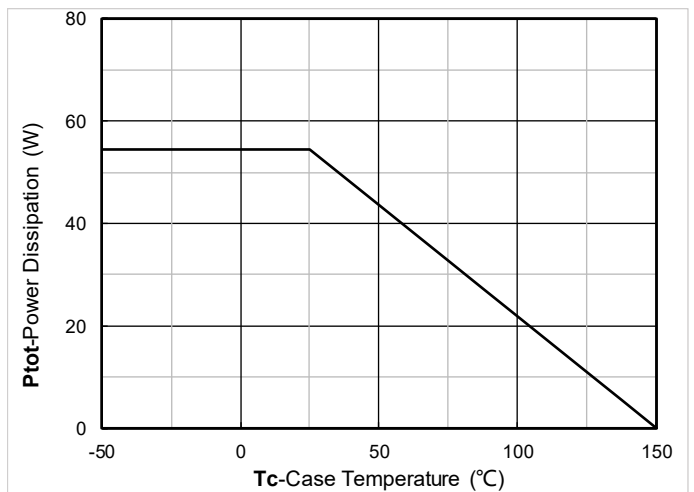


Figure 12. Power dissipation

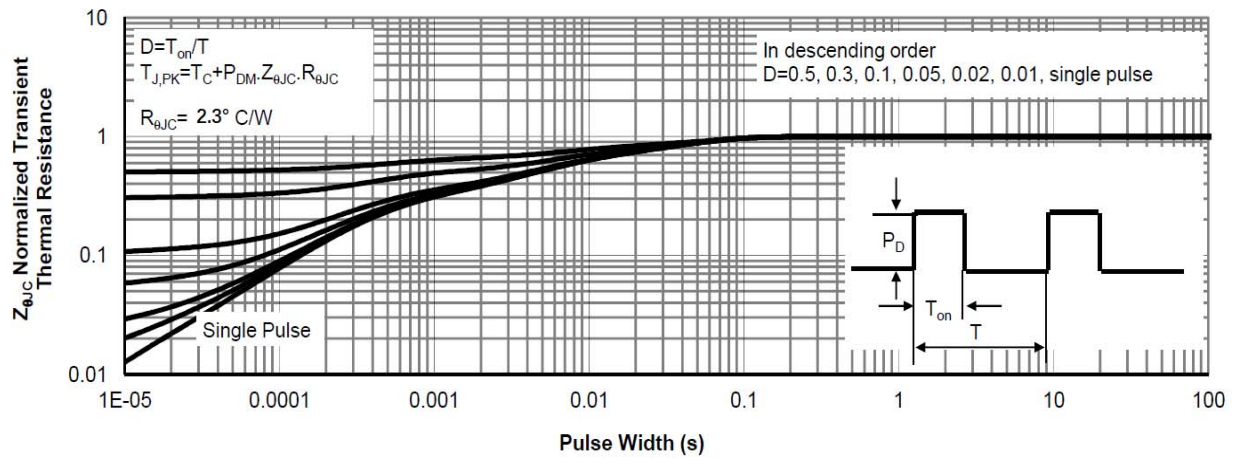
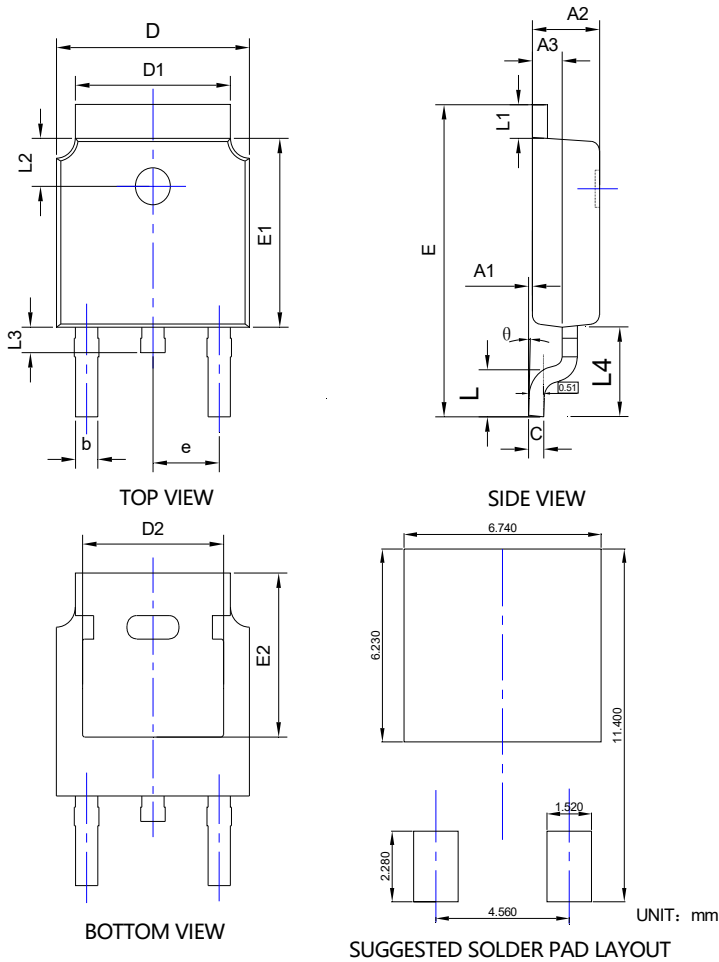


Figure13. Normalized Maximum Transient Thermal Impedance



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■TO-252-B Package information



SYMBOL	DIMENSIONS					
	INCHES			Millimeter		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A1	0.000	---	0.008	0.000	---	0.200
A2	0.087	0.091	0.094	2.200	2.300	2.400
A3	0.035	0.039	0.043	0.900	1.000	1.100
b	0.026	0.030	0.034	0.660	0.760	0.860
c	0.018	0.020	0.023	0.460	0.520	0.580
D	0.256	0.260	0.264	6.500	6.600	6.700
D1	0.203	0.209	0.215	5.150	5.300	5.450
D2	0.181	0.189	0.195	4.600	4.800	4.950
E	0.390	0.398	0.406	9.900	10.100	10.300
E1	0.236	0.240	0.244	6.000	6.100	6.200
E2	0.203	0.209	0.215	5.150	5.300	5.450
e	0.090BSC			2.286BSC		
L	0.049	0.059	0.069	1.250	1.500	1.750
L1	0.035	---	0.050	0.900	---	1.270
L2	0.055	---	0.075	1.400	---	1.900
L3	0.024	0.031	0.039	0.600	0.800	1.000
L4	0.114REF			2.900REF		
θ	0°	---	10°	0°	---	10°

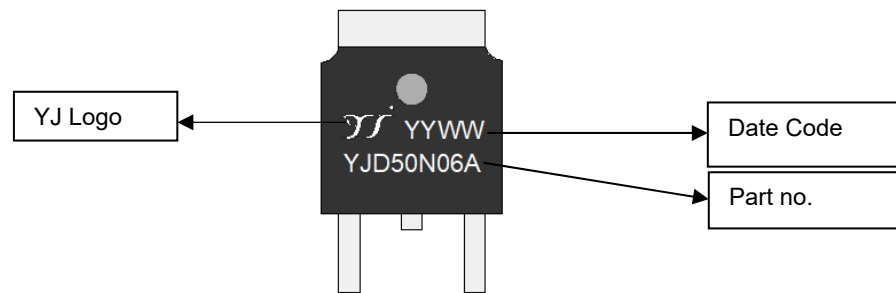
NOTE:

- 1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
- 2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
- 3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.



YJD50N06A

■ Marking Information



Note:

1. All marking is at middle of the product body
2. All marking is in laser printing
3. YJD50N06A is part no., YYWW is date code, "YY" is year, "WW" is week
4. Body color: Black



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